IJERMT

International journal of Engineering Research & Management Technology

ISSN:2348-4039
Volume-1,Issue-1
January 2014

A REPORT ON LOW POWER VLSI CURCUIT DESIGN

Kumar Saurabh **Prashant Mani**
Department of Electronics & Communication Engineering
SRM University, NCR Campus, Ghaziabad, India

ABSTRACT

We survey state-of-the-art optimization methods that target low power dissipation in VLSI circuits. The most important factor in any system design is power. Low power became a major factor where power dissipation has become as important consideration as performance and their area so there is a need of low power. We propose a new family of logic styles called preset Skewed Static Logic (PSSL). PSSL bridges the gap between the two main logic styles, static CMOS logic and domino logic, occupying an intermediate region in the energy-delay-robustness space between the two.. This paper reviews various known strategies and methodologies for designing low power circuits. This paper explains the relation between scaling, power consumption and design robustness.

Key word: PSSL, DS-PSSL, BTBT, DPSCRFF.

INTRODUCTION

In early days, major concern from the designer side was area, performance, cost and reliability [1] power consideration was of only secondary importance. But the scenario is changed in recent few years of vlsi technology these problem were overcome by scaling large circuits into small. This led to another concern which is exponential increases in power consumption which reached optimum level of reliability. But the continuity of scaling into the nanometer, the problem of robustness such as signal integrity and soft error came into effect which poses a great challenge in front of designers. So the aspects related to power consumption and robustness got worse with time. So designers started to think another way so that they can lower the value so power consumption in circuits. Considerations must be at circuit level, because choice of logic style is important because it directly affects power, performance and robustness. There are generally two logic styles they are Static CMOS and domino logic [2].Static CMOS is too slow to be used in timing-critical designs but it is energy efficient and robust. Domino logic though fast, consumes too much power and is not robust. So there is need for new digital logic techniques and style that are simultaneously energy efficient, robust to noise and have high performance. So PSSL [5] (preset skewed static logic) is a new family of logic style. PSSL is better than domino logic in term of robustness and energy. It is better than static CMOS in terms of delay. As PSSL works by partially overlapping. So the execution of consecutive iterations is through speculative evaluation. This is accomplished by presetting nodes at register boundaries before input arrives. Because of this it creates timing slack which can be traded for lower delay and/or lower energy. Another method is a leakage reduction technique in PSSL that takes advantage of slack time to reduce energy delay overhead.

BACKGROUND

Integrated circuit technology has advanced tremendously over the last 40 years, as predicted by Moore's Law[6].Device counts grown exponentially from the 2300 transistors of the Intel 4004 processor in 1971, to the 592 million transistors of the Intel Pentium 2 processor in 2004. Simultaneously clock frequencies have increased exponentially from 0.1MHz in the Intel 4004 to 3.8 GHz in currently shipping Intel Pentium 4's. On the other hand, power consumption has been increasing at 20% per year and has reached power density limits. At the same time, noise, from many sources, as a fraction of power supply voltage, has increased while noise sensitivity has also increased. These factors, together with increased relative process variation and environmental variation, have made predictability and robustness difficult to achieve in new designs.

SOURCE OF POWER DISSIPATION

Power has always been one of the foremost issues in system design. No matter what the design scale, there is a direct correspondence between power dissipation and performance/ functionality, battery life, cost, and size. Power in logic design can be divided into two components as they are dynamic switching and static leakage. Dynamic power dissipation ignore short circuit current which is a small fraction of total dynamic power and it is given by $P=1/CV^2.f$ [7] Where C=average on chip capacitance switched per cycle .V=supply voltage. Sources of power dissipation in CMOS devices are summarized by the following expression [8]

$$\mathbf{P=1/2CV_{DD}^2.F.N+Qsc.Vdd•EN+I_{leak}.V\ dd}$$

Where P denotes the total power Vdd is the supply voltage, and f is f the frequency of operation The first term represents the power required to charge and discharge circuit nodes. Node capacitances are represented by C. The factor N is the switching activity, i.e., the number of gate output transitions per clock cycle. The second term in Eqn. represents power dissipation during output transitions due to current flowing from the supply to ground. The second term in Eqn. represents power dissipation during output transitions due to current flowing from the supply to ground. This current is often called short-circuit current. The factor $\mathbf{Q_{sc}}$ represents the quantity of charge carried by the short-circuit current per transition. The third term in Eqn. represents static power dissipation due to leakage current L_{ai}, . Device source and drain diffusions from parasitic diodes with bulk regions. Reverse bias currents in these diodes dissipate power. Subthreshold transistor currents also dissipate power. In the sequel, we will refer to the three terms above as switching activity power, short-circuit power and leakage current power .The reduction in oxide thickness [4] and threshold voltage has led exponential increase in static leakage power. Static Power dissipation in CMOS circuit is caused by three sources of leakages:1)sub threshold leakage 2)gate leakage 3)band to band tunneling(BTBT) leakage .In these components sub threshold leakage was major component in all leakage at technology larger than 130nm [5].. From the above we can say that power dissipation depends upon physical capacitance so minimizing capacitances offers another technique for minimizing power consumption. Capacitance can be reduced by reducing size of devices, but it also reduces current of transistor which makes its operation slow.

ROBUSTNESS

Robustness [9] is the measure of a design's tolerance to uncertainty. This uncertainty comes from various sources, most importantly from signal noise, single event phenomena (SEP) .Dealing with this noise is the signal integrity challenge. Signal integrity problems manifest primarily in two ways. Firstly, they can directly cause state, such as dynamic nodes, latch nodes, and memory nodes, to be corrupted, causing incorrect computation. Secondly, they can add significant and unexpected delay. Single Event Phenomena and soft errors, is one of the issues affecting the reliability of computing systems Soft errors are the result of SEP (Single Event Phenomena)

CIRCUIT AND LOGIC STYLE

Most common basic logic styles are static CMOS and Domino. A static CMOS logic network is composed of two networks: a pull up network, consisting of PMOS transistor connected to power and a pull down network consisting of NMOS transistor connected to ground. The networks are constructed such that only one network conduct at a particular time in the given set of input. For low fan-in gates in CMOS the power dissipation is less. Transistor sizing in a combinational gate circuit can have significant impact on circuit delay and power dissipation. If the transistors in a given gate are increased in size, then the delay of the gate decreases, however, power dissipated in the gate increases. Further, the delay of the fan-in gates increases because of increased load capacitance. The estimation or analysis of the power consumption of a design is a first step towards incorporating power optimization techniques in a synthesis system. A direct method for power analysis is to translate the given high-level architecture description to the gate, circuit, or physical level; at which point reasonably accurate low-level power analysis tools can be utilized. Disadvantage with static CMOS is that it performs poorly for the most aggressive designs. Domino logic frequently used in high speed design because of the higher performance of dynamic gate. A dynamic logic gate generally differs from the equivalent static CMOS logic gate because the logical effort for each gate is lower. Domino logic frequently used in high speed design because of the higher performance of dynamic gate. A dynamic logic gate generally differs from the equivalent static CMOS logic gate because the logical effort for each gate is lower. The performance of domino logic comes at the cost of power, robustness, and design effort. Domino logic consumes more power because number of transistor increased in output.

PRESET SKEWED STATIC LOGIC

Preset Skewed Static Logic (PSSL) combines the energy efficiency and robustness of static CMOS logic with the performance of domino logic. We first show how Skewed Static Logic can improve performance in the presence of timing slack. We then show how to generate slack through preset. We then show the implementation of PSSL logic and PSSL pipelines. Skewed static logic is a chain of static CMOS inverter. Generally it is a multiple-input multiple output a cyclic combinational circuit which has many activation paths. If there are any differences in delay times between different paths than there is a slack. By resizing transistors, one can often use slack to either increase performance or reduce power dissipation. A simple PSSL circuit resembles the chain of static inverters except that the first inverter has been replaced by NAND gate in which clock is tied in one input.

IJERMT
International journal of Engineering Research & Management Technology
ISSN:2348-4039
Volume-1,Issue-1
January 2014

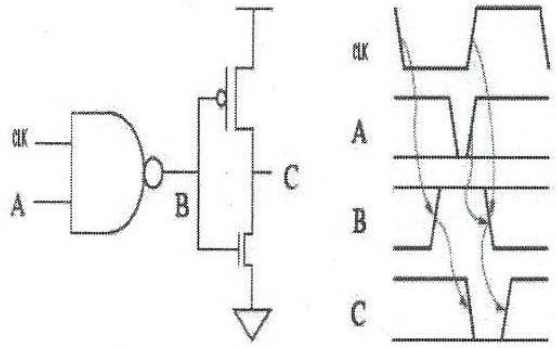
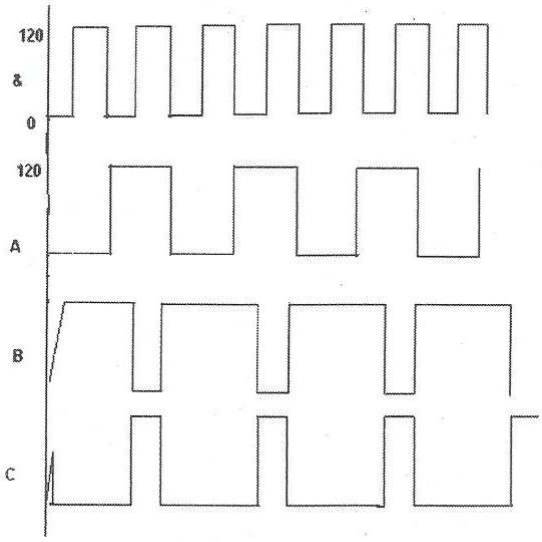


fig :Preset Skewed Static Logic. Smaller transistors are less critical.



Timing diagram

Firstly falling edges of clock initiate the process of preset. In this time all circuit nodes are indirectly forced to pre-determined values. In particular, node B raises in turn causing node C to fall. The idea behind the preset process is that we are computing all the nodes of the circuit presuming low input values. This begins one clock phase before the actual put value(s) arrive, so this computation has an extra clock phase to complete. The rising edge of the clock initiates the process of evaluate. The process of evaluate is independent of the process of preset, and in particular, evaluate can begin before preset completes. If the value of the input node, A is low at the rising edge of the clock and remains low, nothing happens and evaluate is complete. However, if the input node A, is high when the clock rises or node A rises while the clock is high, then it causes node B to fall in turn causing node C to rise, completing the evaluate process. Whether node A is high or low, eventually node C gets the correct value. However, we have decoupled the computation for low values of A (the preset process) from the computation for high values of A (the evaluate process), giving the former computation extra time and thus creating slack in the path of transistors in the preset process (i.e. the preset path).We can take advantage of this slack by reducing the size of transistors in the preset path to reduce power consumption or by increasing the size of transistors in the evaluate path to reduce delay. Preset allows PSSL to

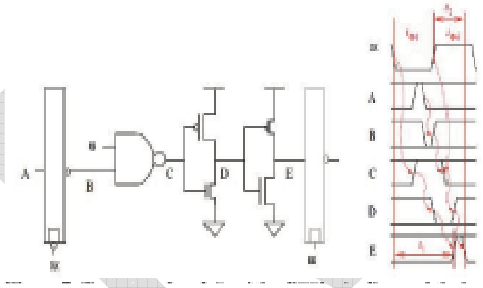
outperform generic static CMOS logic. However preset comes at the cost of extra power consumption because of spurious transitions from input mis-speculation and extra clocking overhead.

PIPELINING

Now we examine how to create pipelines using PSSL. PSSL using the three major clocking schemes: level-sensitive, edge-triggered, and pulse

Level-sensitive

Level-sensitive clocking uses alternating transparent latches as timing elements. A two phase Level-Sensitive PSSL (LS-PSSL) pipeline, shown in Figure is the composition of PSSL pipeline stages of alternating phase, separated by transparent latches. One stage begins preset when adjacent stages begin evaluate. In LS¬PSSL, the transparent latches serve two purposes. First, they hold pipeline state. Every legal pipeline must have at least one latch in each full pipeline stage. Second, the latches prevent the preset wave-front from propagating to the following stage until after the preset phase. Otherwise, if the wave-front propagates early, it will cause inter-symbol interference as it becomes indistinguishable from the evaluate wave-front from the previous cycle.



The operation of LS-PSSL, shown in Figure as follows. The falling edge of the clock begins preset, causing C to rise, D to fall, and finally E to rise. This path, whose delay is t1, must complete in one clock cycle, less setup delay. This coincides with the closing of the second latch at the falling edge of the clock. Therefore we derive the constraint

$$ti + ts < tch + tct$$

where ts is the setup time of the latch . The rising edge of the clock begins evaluate. The value of A is effectively sampled by the first latch and NAND gate combination at the rising edge of the clock. If it is low, then C falls, D rises, and, finally, E falls. This path, whose delay is t2, must complete one setup delay before the closing edge of the latch. Therefore we derive the constraint t2+ ts < to Similarly, the equations of the other half of the pipeline (not shown) are given by t3+ ts < tci + to + ts < tci The preset path delays, ti and t3 can be twice as long as the evaluate path delays, t2 and ta. As opposed to level-sensitive clocking, edge-triggered clocking uses a single monolithic timing element (usually a flip-flop). Figure 6 shows a pipeline using the same latch and NAND gate combination as before. However, this time there is only one set in a full pipeline stage, along with the diagram. The corresponding timing constraints are

$$ti + ts < to + 2td$$
$$t2\ ts < tch\ tcl\ t1 > tc$$

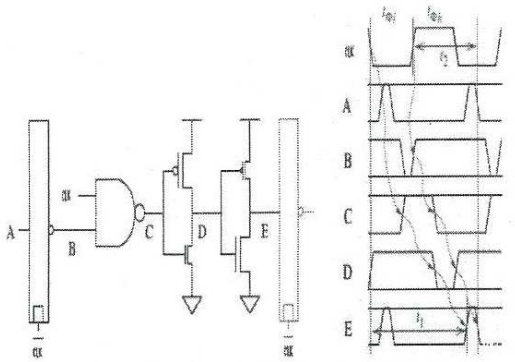


Figure Edge Triggered PSSL and timing diagram.

The timing paths being and end on clock edges so that there is no time borrowing allowed. Note that there is a minimum path delay constraint on clock phase 2. Violating this constraint would cause inter-symbol interference. This is a fundamental race condition that cannot be avoided

CONCLUSION

PSSL is an ideal technology to cope with scaling issues. It is more robust than domino because of its reduced reliance on dynamic logic it becomes harder to use dynamic logic as technology scales because of increased noise and decreased Noise-immunity. PSSL uses dynamic logic gates, not for its lower logical effort, but for its preset, which can be used to speed up all the downstream logic. Therefore, the reduced performance of dynamic logic due to scaling becomes unimportant.

REFERENCES:

1 Gordon E. Moore. Cramming more components onto integrated circuits. Electronics, 38(8), April 1965.
2 Kaushik Roy, Saibal Mukhopadhyay, and Hamid Mahmoodi- Meimand. Leakage current mechanisms and leakage reduction techniques in deepsubmicrometer CMOS circuits. Proc. IEEE, 91(2):305-327, February 2003.
3 Saibal Mukhopadhyay, Arijit Raychowdhury, and Kaushik Roy. Accurate estimation of total leakage in nanometer-scale bulk CMOS circuits based on device geometry and doping profile. IEEE Trans. Computer-Aided Design of
4 Integrated Circuits and Sytems, 24(3):363-381, March 2005.
5 A. Agarwal et al."Leakage power analysis and reduction: models, estimation and tools"IEEE Proc. Comput.Digit. Tech., 152(3):353-368, May 2005.
6 Arjit Raychowdhury, SaibalMukhopadhyay, and Kaushik Roy. "Modeling and estimationof leakage in sub90nm devices" In Int. Conf. VLSI Design, pages 65-70, 2004.
7 Gordon Moore "No exponential is forever but forever can be delayed" In ISSCC,pages 20-23, February 2003.
8 OfridiWechsle"Inside Intel Core microarchitecture. technology/new architecture 06.pdf.
9 Samuel K. H. Fung et al. "65nm CMOS high speed, general purpose and low powertransistor technology for high volume foundry application" In Symp. VLSI Tech., pages92-93,2004.
10 Rajeev R. Rao et al. "Parametric yield estimation considering leakage variability" InDAC, pages 442-447, June 2004.
11 Yibin Ye, Shekhar Borkar, and Vivek De. A new technique for standby leakage reduction in high-performance circuits. In Symp. VLSI Circuits, pages 40— 41, June 1998.
12 M. C. Johnson, D. Somasekhar, and K. Roy. Leakage control with efficient use of transistor stacks in single threshold CMOS. In DAC, pages 442-4-45,1999.
13 Walid Elgharbawy et al. On gate leakage reduction in dynamic CMOS circuits. In Midwest Symp. Circ. Syst.,pages 1390-1393,2005.

14 Shin'ichiro Mutoh et al. 1-V power supply high-speed digital circuit technology with multi threshold-voltage CMOS. IEEE J. Solid-State Circuits, 30(8):847-854, August 1995