International Journal of Engineering Research & Management Technology ISSN: 2348-4039

Email: editor@ijermt.org September - 2014 Volume 1, Issue-5 www.ijermt.org

Cascaded Multilevel Inverters with Finest Switching Sequence for High Power Applications

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ABSTRACT

This work presents simulation of cascaded multilevel inverter with optimal switching sequence for high power applications. Certain Sequential Switching Hybrid Modulation strategies and designed for performance of the well-known alternative phase opposition disposition (APOD) is presented here. The main characteristic of these modulations are the reduction of switching losses with better harmonic performance. A simple sequential switching and base pulse-width modulation (PWM) circulation techniques are embedded with these modulations, to achieve balanced power dissipation among the devices within a cell and for series connected cells, equal load sharing. A detailed harmonics analysis is done on the single phase five level cascaded type voltage source multilevel inverter.

Keywords— cascaded MLI , optimal switching sequences, switching loss , harmonics analysis, equal power dissipation .

I. INTRODUCTION

The concept of multilevel converters has been introduced since 1975.The term multilevel began with the 3-level converter. **M**ULTILEVEL inverters (MLIs) are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high-power applications, because improving the output waveform of the inverterreducesit

Respective harmonic content and hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation [1]. The output of conventional two-level inverter is in the form of square wave ac power which usually contains undesirable harmonics [6]. When this output is fed to an electrical device such as an electrical motor it causes heating which in turn causes increased losses and finally resulting in decreased efficiency [2]. This is caused by high harmonic contents. These harmonics increases the total harmonic distortion value which is responsible for reducing the quality of output. The harmonics has to be removed in order to attain a proper sine wave. The harmonics in the output side of the inverter can be eliminated using multi level inverter structures. MLIs can operate by Hybrid modulation techniques such as combination of Fundamental Switching Frequency Modulation (FPWM) **a**nd High Switching Frequency Modulation MSPWM for each inverter cell operation. Most of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulse width modulation (PWM).The carriers can be arranged with vertical shifts (phase disposition, and alternative phase opposition disposition (APOD) PWM), or with horizontal displacements (phase-shifted carrier (PSC) PWM).

From the various literature surveys, it has been found that cascaded multilevel inverter is more suitable for high power applications such as STATCOM in transmission lines, A.C Drive application in industries. The multilevel inverter can operate at both fundamental switching frequency and high switching frequency PWM. Subsequently, several multilevel converter topologies have been developed. Cascaded H bridge inverter is one of the most

important topologies in multilevel inverters Capacitor, Battery and Renewable Energy voltage source can be used as the multiple d.c voltage sources [1] d.c sources are connected in series which is shown in Fig 1. The performance of symmetrical CHB multilevel inverter with respect to harmonic content, number of switches and voltage stress across the switch is calculated by using MATLAB/Simulink Software.

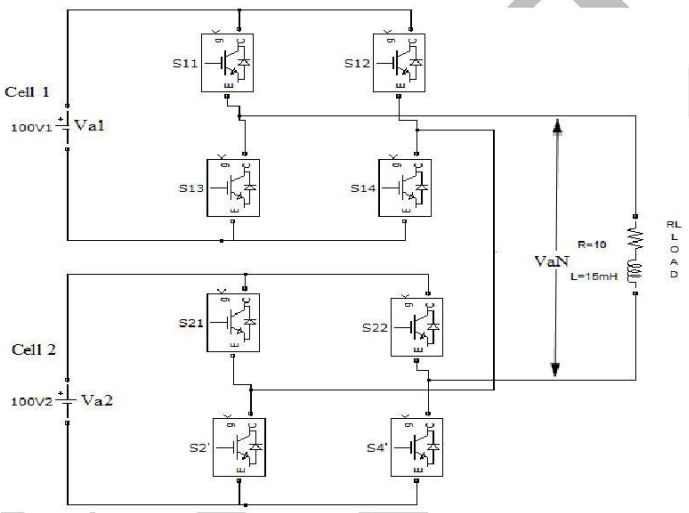


Fig 1. Block diagram of Cascaded H bridge inverter

II. PROPOSED SCHEME

A. Review of MSPWM schemes

The major MSPWM scheme, Alternative Phase Opposition Displacement (APOD) shows efficient Performance analysis of PWM strategies [1]. Unipolar carrier-based N-level PWM operation consists of (N − 1)/2 different carriers, same as the number of FBI cell (K = (N − 1)/2). The carriers have the same frequency fc, the same peak-to-peak amplitude Ac, and disposed. For APOD, all carriers are phase opposition by 180◦ from its adjacent carrier shown in Fig 2.

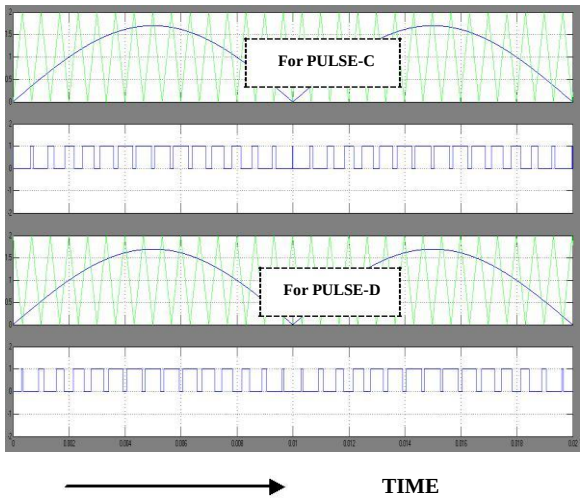


Fig 2. Sinusoidal reference and carriers of MSPWM operation of APOD

B. Need of Effi cient Hybrid Modulation Techniques

The main aim of the project is to reduce the switching loss of multilevel sinusoidal modulation (MSPWM) schemes with low computational overhead. Also, it covers the methodology for equal power dissipation among the power devices, and the power modules. Although only the five-level CMI case is presented here shown in Fig 1, the proposed method can be equally applied to any number of voltage levels with any number of phases. In the recent 15 years, however, there has been growing awareness that electromagnetic interferences (EMI) were affecting the human body. Most notable was the concern that cellphone usage and high power lines caused cancers and diseases. For 4 Billion years, life on earth has been in an EMI free environment, shielded by the earth magnetic field. Many scientists believe that life faced great challenges when the magnetic field naturally weakened over the millions of years. So EMI protection is essential for the Biosphere. It is the author's opinion that EMI plays a great role in the mental health of populations and might be affecting history. Electronic equipment can malfunction or become totally inoperable if not designed to properly minimize the effects of interference from the internal and external electromagnetic environments. Proper equipment and system designs are also necessary for minimizing potential electromagnetic emissions into the operating environment The Efficient Sequential Switching Hybrid Modulation Techniques are the proper system design for minimizing potential electromagnetic emissions with better harmonic performance. In order to achieve a wide range of modulation indexes with minimized THD for the synthesized waveforms

III. BLOCK-DIAGRAM EXPLANATION OF THE PROPOSED SCHEME

Methods that work with high switching frequencies have many commutations for the power semiconductors in one period of the fundamental output voltage. Methods that work with low switching frequencies generally perform one or two commutations of the power semiconductors during one cycle of the output voltage, generating a staircase waveform. Several research works has been going on for past twenty years in selecting and designing a suitable converter for High Power application. Multilevel Inverters are found to be more suited for Industrial applications. Several modulation techniques exist for the inverters. The various surveys done on modulation techniques are summarized in this chapter. The results show that multilevel inverter can operate at both fundamental switching frequency and high switching frequency PWM.

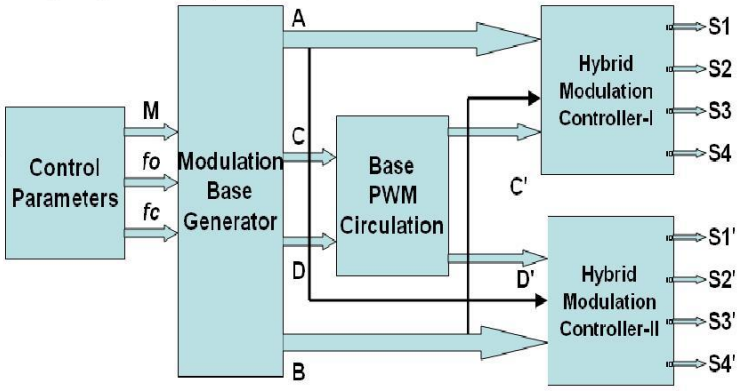


Fig 3 Block diagram of proposed sequential switching hybrid modulation

Basic Principle Hybrid modulation is the combination of fundamental frequency modulation (FPWM) and MSPWM for each inverter cell operation, so that the output inherits the features of switching-loss reduction from FPWM, and good harmonic performance from MSPWM. In this modulation technique, the four switches of each inverter cell are operated at two different frequencies; two being commutated at FPWM, while the other two switches are modulated at MSPWM, therefore the resultant switching patterns are the same as those obtained with MSPWM. A sequential switching scheme is embedded with this hybrid modulation in order to overcome unequal switching losses, and therefore, differential heating among the power devices. A simple base PWM circulation

scheme is also introduced here to get resultant hybrid PWM circulation makes balanced power dissipation among the power modules Fig. 3 shows the general structure of the proposed SSHM scheme. It consists of modulation base generator, base PWM circulation module, and hybrid-modulation controller (HMC) to generate new modulation pulses.

A. Control parameters

The modulation index for MSPWM is defined as M = Am/K(Ac) and K = (N − 1)/2 where N=no of levels . The modulation frequency ratio is given as mf = fc/fo , where Control parameters M,f0,fc are M – modulation index(0.85), f0 – fundamental frequency(50HZ), fc – carrier frequency(1.5kHZ), Ac-carrier amplitude, Am-modulated signal amplitude.

B. Base-Modulation Generator Design

In this modulation strategy, three base-modulation pulses are needed for each cell operation in a CMLI. A sequential switching pulse (SSP) (A) is a square-wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM, and FPWM sequentially to equalize the power losses among the devices. FPWM (B) is a square-wave signal synchronized with the modulation waveform; B = 1 during the positive half cycle of the modulation signal, and B = 0 during negative half cycle. An SSP and FPWM pulses are same for all inverter cells. MSPWMs (C or D) for each cell, differs depends upon the type of carrier and modulation signals used. The block diagram representation of base modulator design is shown Fig 4.

(a)–(d).APOD modulation pulses for cell-I (C) is obtained from the comparison between unipolar modulation waveform and carrier, while APOD for cell-II (D) is generated from the comparison between modulation waveform and carrier with d.c bias of−Vc + 2Ac .

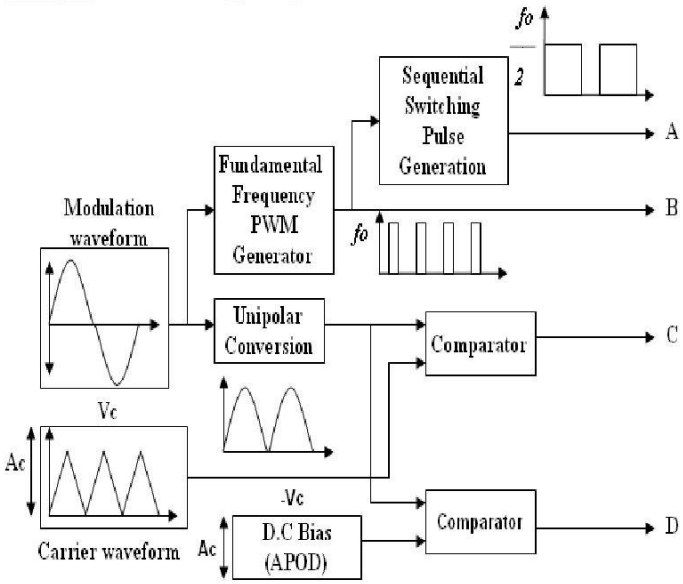


Fig 4. Block model of five-level base modulator for APOD

C. Base PWM Circulation

A simple base PWM circulation scheme introduced here to get resultant HPWM circulation among the power modules shown in Fig 5, consists of two 2:1 multiplexer, and selects one among the two PWMs based on the select clock signal. The clock frequency is fo/4, makes the time base for PWM circulation from one module to another. After two fundamental frequency periods, the order is changed so that the first module HPWM becomes the second module, the second becomes the third, etc., while the last module HPWM shifts to the first.

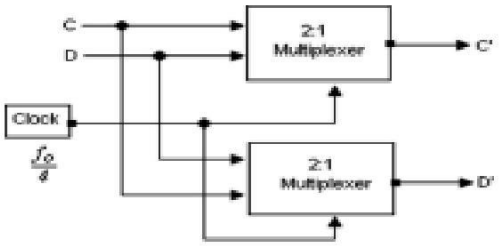


Fig 5. Scheme of base PWM circulation of five-level cascaded multilevel inverter

D. Hybrid-Modulation Controller

HMC combines SSP, FPWM, and MSPWM that produces SSHM pulses. It is designed by using a simple combinational logic and the functions for a five-level HPWM are expressed as

$$S1 = ABC' + \overline{A}B \qquad S1' = ABD' + \overline{A}B$$
$$S2 = A\overline{B}C' + \overline{A}\,\overline{B} \quad \text{and} \quad S2' = A\overline{B}D' + \overline{A}\,\overline{B}$$
$$S3 = \overline{A}\,\overline{B}C' + A\overline{B} \qquad S3' = \overline{A}\,\overline{B}D' + A\overline{B}$$
$$S4 = \overline{A}BC' + AB \qquad S4' = \overline{A}BD' + AB$$

Where A is an SSP, B is an FPWM, C_ is an MSPWM for cell-I and D_ is an MSPWM for cell-II. In Fig. 8, it is shown that each gate pulse is composed of both FPWM and MSPWM. If SSP A = 1, then S1, S2, S1_, andS2_ are operated with MSPWM, while S3, S4, S3_, and S4_ are operated at FPWM. If SSP A = 0, then S1, S2, S1_, and S2_ are operated at FPWM, while S3, S4, S3_, and S4_ are operated with MSPWM. Since A is a sequential signal, the average switching frequency amongst the four switches is equalized. Voltage stress and current stress of power switches in each cell is inherently equalized with this modulation. After every two fundamental periods, the HPWM pattern is changed so that the first module (S1, S2, S3, and S4) becomes the second module (S1_, S2_, S3_, and S4_), and the second one shifts to the first, and is shown in Fig. 8

IV. SIMULINK RESULT OF PROPOSED MODULE

The multilevel inverter can operate by Hybrid Modulation strategies. Then the performance of symmetrical CHB multilevel inverter with respect to harmonic content, number of switches and voltage stress across the switch is calculated by using MATLAB/Simulink Software. A detailed harmonics analysis is done on the CHB-MLI by considering 5-level operation which is shown in Fig 6.

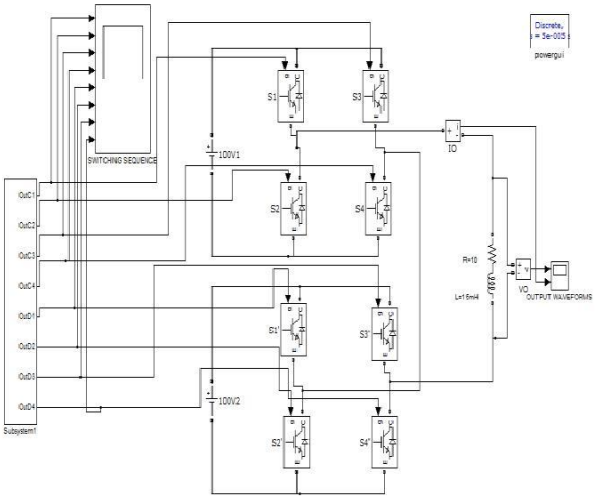


Fig 6. Simulink model of CMLI for Proposed System

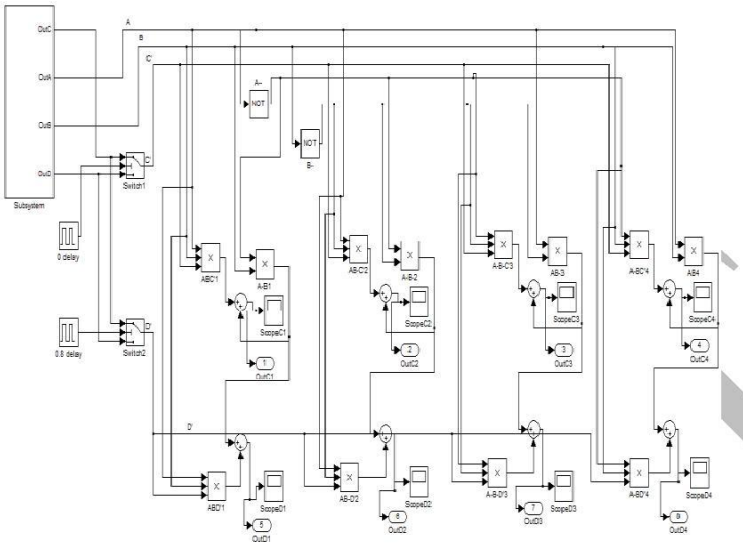


Fig 7. Simulink model of sequential switching hybrid modulation Techniques

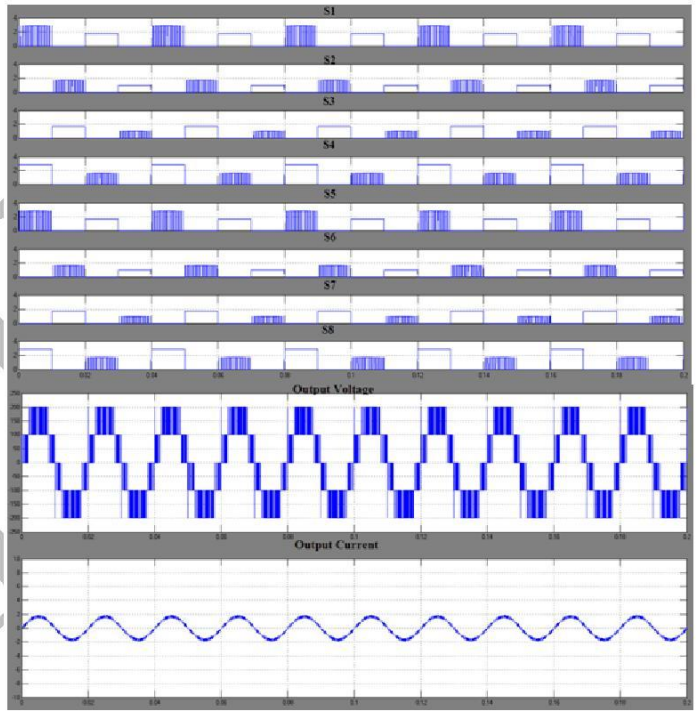


Fig 8. Five-level switching sequence of pulses

The waveforms of output voltage, the implementation of HPWM circulation makes the inverter modules operate at same average switching frequency with the same conduction period. As a result, all inverter cells operate in a balanced condition with the same power-handling capability and switching losses is shown in Fig. 8

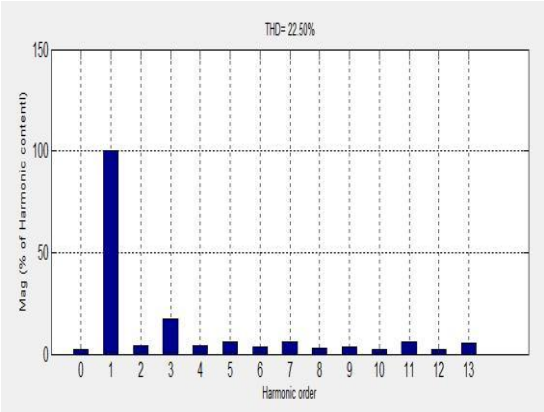
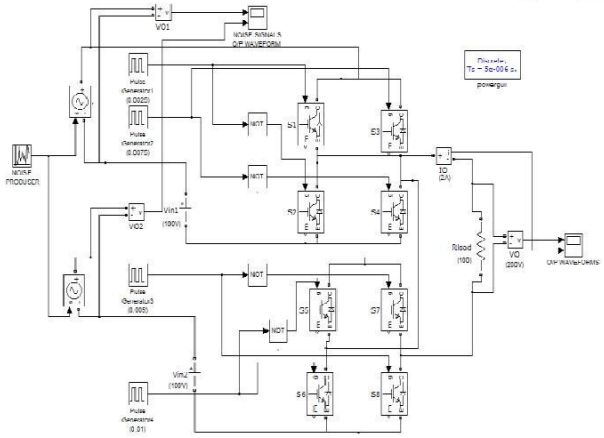


Fig 9. Spectral analysis of output voltage waveform

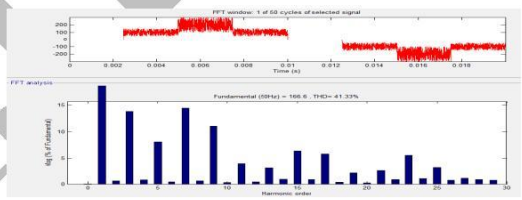
To evaluate the quality of the output voltage waveforms, the values of total harmonic distortion (THD) is calculated up to 50th order of harmonics, as suggested in the IEEE standard 519. The harmonic spectrum of output voltage waveform of five level inverter is shown in the Fig 8 and the %THD (0.2256) value measured using FFT block are shown in Fig 9.

V. EFFECT OF THD IN VARIOUS MODULE

For APOD, we can observe that there is a significant reduction in the THD content compared to the fundamental frequency techniques(%THD)[1] which is proved by comparing THD effect on Existing and Proposed System shown in Fig 10(a)-(b) and Fig 11(a)-(b).

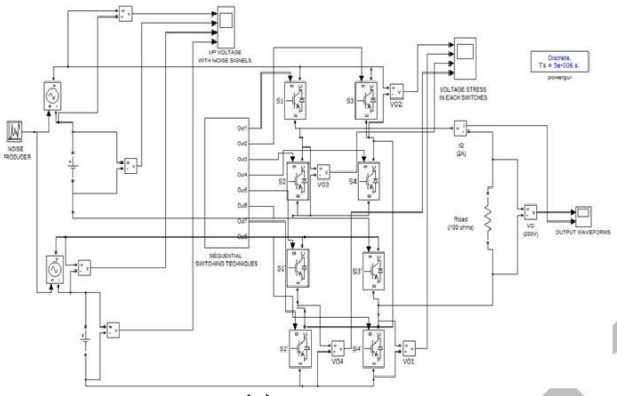


(a)

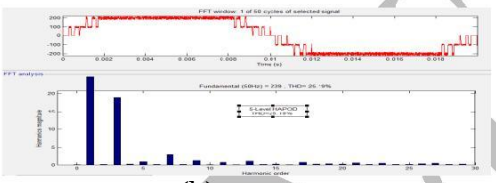


(b)

Fig 10. Simulink result of Existing System: (a) Block model of Cascaded multilevel inverter with disturbance, (b) Spectrum value



(a)



(b)

Fig 11. Simulink result of Proposed System: (a) Block model of Cascaded multilevel inverter with disturbance, (b) Spectrum value

The spectrum analysis should be observed that for proposed module (HAPOD), the voltage harmonics (%THD=25.19) is less when compared with existing module (fundamental frequency techniques) THD is 41.33% with better harmonic performance.

VI. HARDWARE ELEMENTS AND ITS DESCRIPTION

A. Regulator IC's-7805, 7812

The power supply section is the important one. It should deliver constant output regulated power supply for successful working of the project. A 0-12V/1mA transformer is used for this purpose. The primary of this transformer is connected in to main supply through on/off switch& fuse for protecting from overload and short circuit protection. The secondary is connected to the diodes to convert 12V AC to 12V DC voltage. And filtered by the capacitors, which is further regulated to +5V, by using IC7805 and to +12V by using IC7812 which is used for the supply for microcontroller (40-pin IC) and for the MOSFET gate driver (14-pin IC).

B. Micro Controller- PIC 16F877A

Peripheral Details: Timer0: 8-bit timer/counter with 8-bit prescaler, Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock, Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler, Two Capture, Compare, PWM modules, Capture is 16-bit max, resolution is 12.5 ns Compare is 16-bit max, resolution is 200 ns, PWM max, resolution is 10-bit Synchronous Serial Port (SSP) with SPI (Master mode) and I2C (Master/Slave), Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection, Parallel Slave Port (PSP) – 8 bits wide with external RD, WR and CS controls (40/44-pin only), Brown-out detection circuitry for Brown-out Reset (BOR).

Special Microcontroller Applications: 100,000 erase/write cycle Enhanced Flash program memory typical, 1,000,000 erase/write cycle Data EEPROM memory typical, Data EEPROM Retention > 40 years, Self-reprogrammable under software control, In-Circuit Serial Programming via two pins, Single-supply 5V In-Circuit

Serial Programming Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation Programmable code protection, Power saving Sleep mode, Selectable oscillator options, In-Circuit Debug (ICD) via two pins.

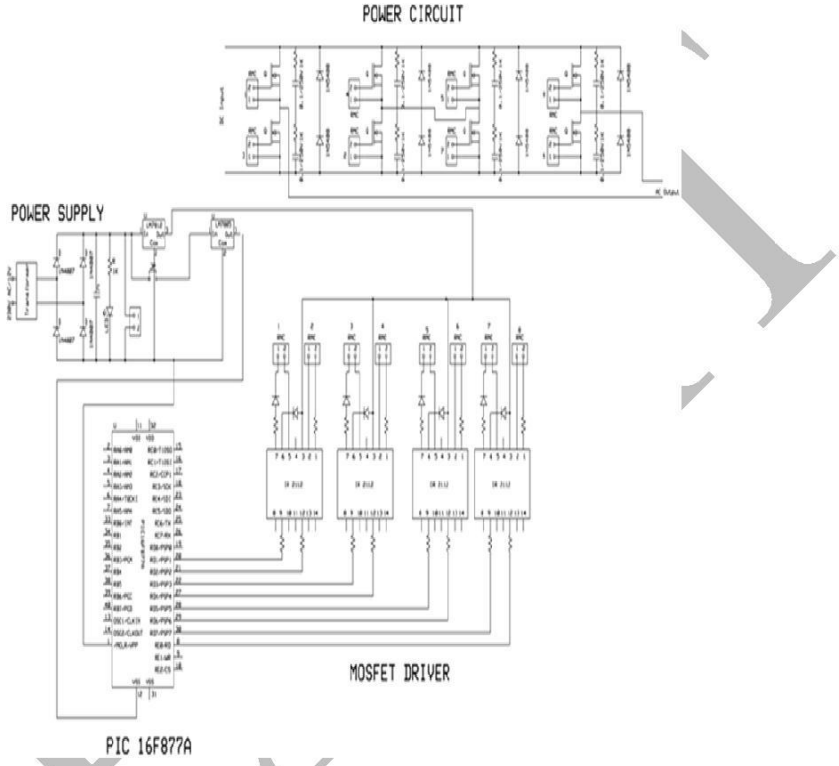


Fig 12 . Hardware model of proposed system

C. MOSFET-IR840

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters and motor drivers.

D. RL load: Resistor-(10K, 47,470) ohm, Inductor-15mH

In this section, successful applications of CHB inverters are presented. The application has particular requirements where cascaded inverters are well suited. There are several suppliers of CHB inverters in the market of medium-voltage drives [8].

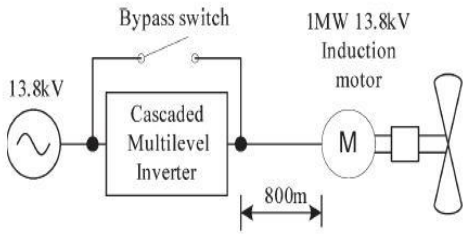


Fig 13. Cascaded Multilevel Inverter application: Pumps and Fans

Pumps and fans are intensively used in almost all industry sectors shown in (Fig 13). High-voltage high-power pumps and fans are used in water plants, oil and gas plants, cooling systems, geothermal and nuclear power plants, underground mining, furnaces and boilers, and so on.

CONCLUSION

This paper has provided a brief analysis of cascaded multilevel inverter circuit topologies and a new family of SSHM techniques for CMLI, operating at a lower switching frequency is proposed. Compared to conventional MSPWM schemes, switching-loss reduction is obtained and the harmonic performance of the SSHM schemes are analyzed in the entire range of modulation index and it seems to be good. The proposed technique is applied to well-known MSPWM schemes called APOD. As a result of proposed system, Switch working under ZVS condition and resonant condition also achieved. An early patent for the cascaded multilevel inverter can be traced back to 1975. However, the commercial products that utilize this superior circuit topology were not available until the mid-1990s. Today, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring.

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