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COMPARISON AND ANALYSIS OF TOTAL HARMONIC DISTORTION IN CASCADED MULTILEVEL H-BRIDGE INVERTERS FOR INDUCTION MOTOR DRIVE APPLICATION

Ankit Kumar
SVS University
Meerut

Smrati Singh
SRM University
Modinagar

D.V.Avasthi
SVS University:
Meerut

ABSTRACT

Multilevel inverter technology has emerged recently as a very important alternative in the areas of high-power medium-voltage energy control and drive applications. Theoretically, a multilevel inverter can be envisioned as a voltage synthesizer, in which the high output voltage is realized from many discrete smaller voltage levels. This new power conversion strategy allows devices with low dv/dt capability and low switching frequencies to successfully operate medium and high power circuits with high power efficiency in a large variety of applications.

This research aims to analyze and compare total harmonic distortion in cascaded three level and modified five level h-bridge inverters and evaluate THD in the respective outputs. Effort is made to minimize hardware requirement and output THD of the multilevel inverter circuits. Some useful results obtained from the MATLAB simulation are also presented.

Indexing terms: Multilevel Inverters (MLIs), Total Harmonic Distortion (THD), Electromagnetic Interference (EMI)

MUTILEVEL INVERTER

Multilevel inverters (MLIs) are becoming more popular now a days due to their advantages over conventional three-level pulse width modulated (PWM) inverters. MLIs offer improved output waveforms, smaller filter size, low EMI, and lower total harmonic distortion (THD) etc. Figure 1 shows One phase leg of an inverter with two levels, three levels, and n level switching.

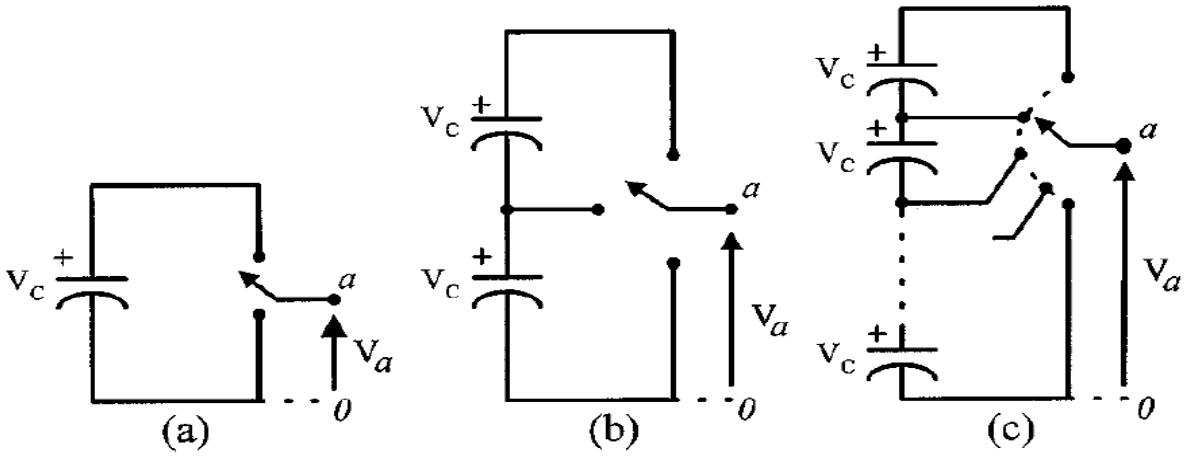


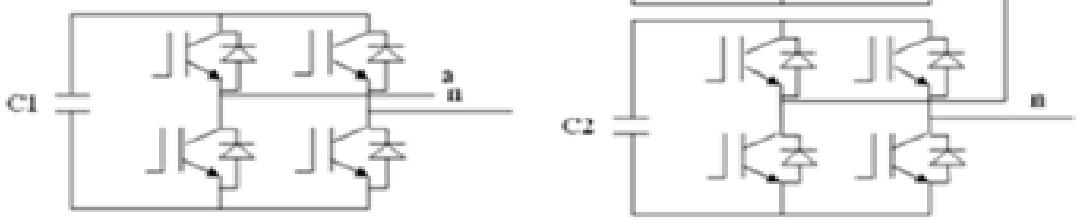
Fig 1. One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels.

Multilevel inverter topology can be designed for the least number of components for a given number of levels. Cascaded H-Bridge-MLI topology is based on the series connection of H-bridges with separate DC source for each bridge. Since the output terminals of the H-bridges are connected in series, the DC sources must be isolated from each other. The need of several sources on the DC side of the inverter makes multilevel technology attractive for photo voltaic applications. Essentially, the main attraction of Cascaded H-Bridge-MLIs lies in modularized layout and packaging of H-Bridge cascade and larger number of ac voltage output levels m for a given number of dc input voltage levels s (m=2s+1). Each H-bridge requires a separate dc source (SDC), which is a disadvantage of H-bridge limiting its application to products that already have multiple SDCs readily available.

The Single-phase structure of a multilevel cascaded H-bridges inverter is shown in figure (2). The Fourier Transform for phase voltage van = va1 + va2 + va3 + va4 + v a5 for a stepped waveform such as the one depicted in Figure 2 with s steps may be written as

$$H(n)=\frac{4}{\pi n}\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right], \quad \text{where } n = 1, 3, 5, 7, \ldots$$

The conducting angles θ_1, θ_2,. θ_3..s can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th , harmonics are eliminated.



(a) (b)

Fig 2. Single phase structure of multilevel cascaded H-bridge inverter (a) three level (b) five level

As in the single phase voltage source inverters PWM technique can be used in three-phase inverters, in which three sine waves phase shifted by 120° with the frequency of the desired output voltage is compared with a very high frequency carrier triangle, the two signals are mixed in a comparator whose output is high when the sine wave is greater than the triangle and the comparator output is low when the sine wave or typically called the modulation signal is smaller than the triangle. This phenomenon is shown in Figure 1 as is explained the output voltage from the inverter is not smooth but is a discrete waveform and so it is more

likely than the output wave consists of harmonics, which are not usually desirable since they deteriorate the performance of the load, to which these voltages are applied.

Recent advances in power electronics have made the multilevel concept practical. In fact, the concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operation. Multi-level inverters are the modification of basic bridge inverters. They are normally connected in series to form stacks of level. The number of levels in an inverter bridge defines the number of direct current (DC) voltage steps that are required by the inverter bridge in order to achieve a certain voltage level at its output.

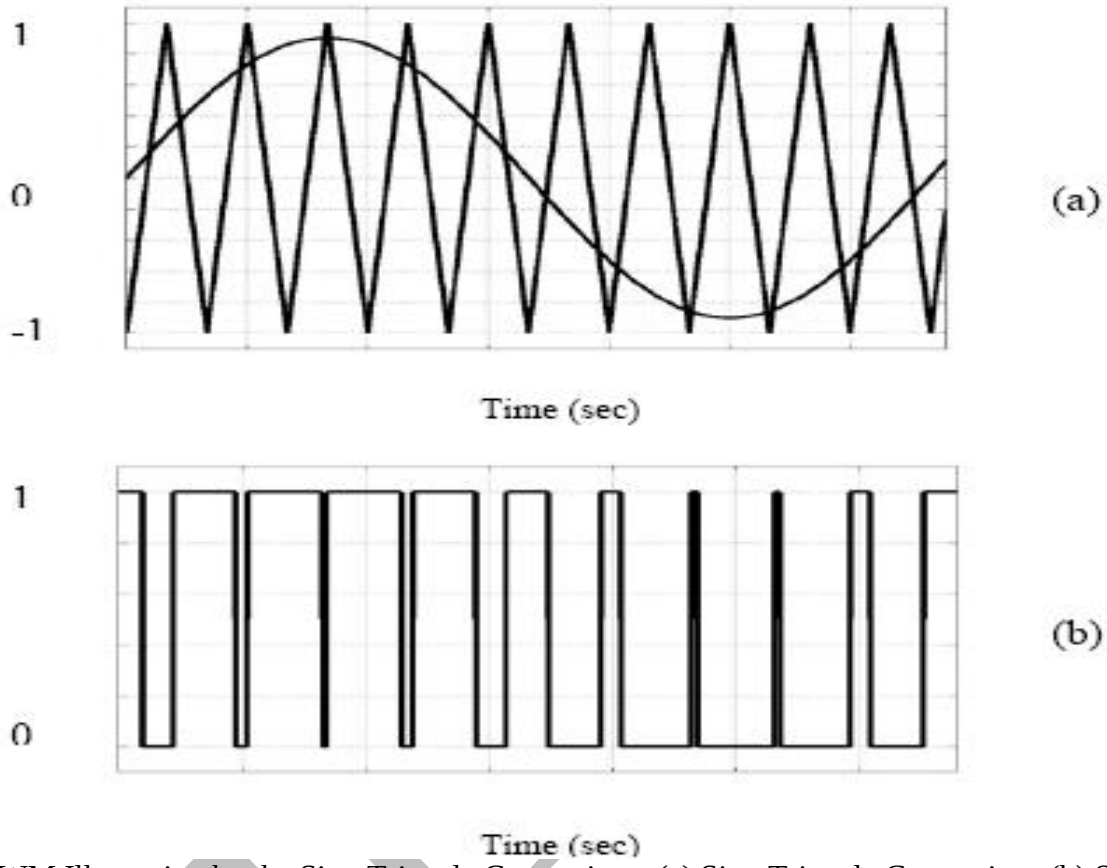


Fig (3).PWM Illustration by the Sine-Triangle Comparison: (a) Sine-Triangle Comparison (b) Switching Pulses

The advent of the transformer less multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter. The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters. In this method, a fixed D.C. input voltage is supplied to the inverter and a controlled A.C. output voltage is obtained by adjusting the on and–off periods of the inverter devices. Voltage-type PWM inverters have been applied widely to such fields as power supplies and motor drivers. This is because: (1) such inverters are well adapted to high-speed self-turn-off switching devices that, as solid-state power converter provided with recently developed advanced circuits; and (2) they are operated stably and can be controlled well.

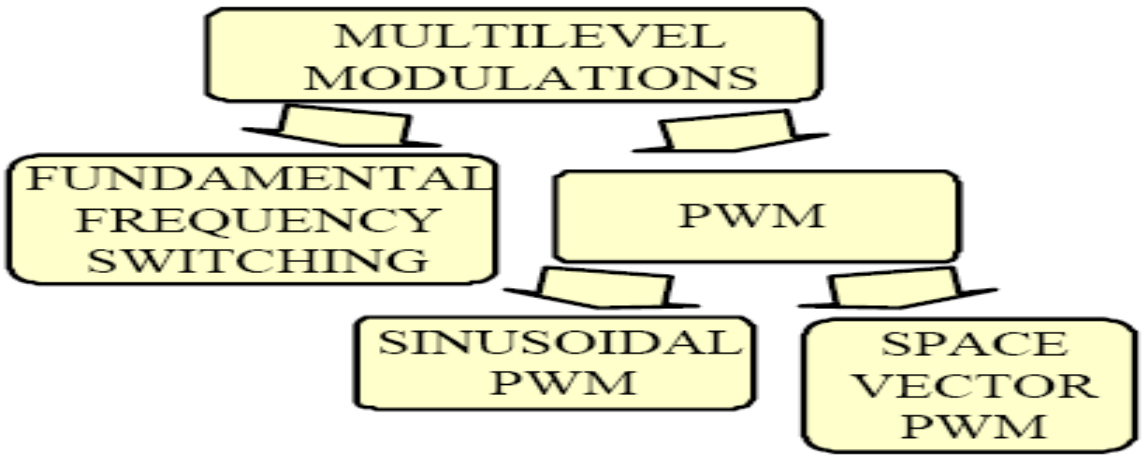


Figure 4: Multilevel Modulation Techniques

From the above mentioned PWM control methods, the Sinusoidal pulse width modulation (SPWM) is applied in the proposed inverter since it has various advantages over other techniques. Sinusoidal PWM inverters provide an easy way to control amplitude, frequency and harmonics contents of the output voltage. Sinusoidal pulse width modulation (SPWM) is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. In the modulation techniques, there are two important defined parameters:-

a. the ratio P = fc/fm known as frequency ratio, and
b. the ratio Ma = Am/Ac known as modulation index,

Where fc is the reference frequency, fm is the carrier frequency, Am is reference signal amplitude and Ac is carrier signal amplitude. For NPC multilevel inverters, most carrier based modulation strategies derive from disposition techniques developed by Carrara et al, where for an M level inverter, M1 carriers of identical frequency and amplitude are arranged to occupy contiguous bands between +VDC and -VDC.

- Alternative Phase Opposition Disposition (APOD), where each carrier is phase shifted by 1800 from its adjacent carriers.
- Phase Opposition Disposition (POD) where the carriers above the reference zero point is out of phase with those below the zero point by 1800.
- Phase Disposition (PD).

MODIFIED CASCADED FIVE LEVEL INVERTER

In Modified cascaded five level inverter an auxiliary circuit is added in the simple H-Bridge inverter. The output voltage of simple H- Bridge inverter is the three level voltage waveform, to make it a five level wave the auxiliary circuit is connected, which contains two back-to-back IGBT switches in series with the diodes. Fig 5 shows a new five level inverter for single phase.

For $+V_{dc}/2$ switches S_4 and S_6 is on and for $+V_{dc}$ switches S_1 and S_4 is on and for $-V_{dc}/2$ switches S_2 and S_3 is on and for $-V_{dc}$ switches S_2 and S_5 is on and for zero either switches S_4,S_1 or switches S_2,S_4 is conduct.Therefore, five level inverter output voltage is obtained. Sinusoidal PWM law has been adopted to generate the gating pulses for modified five level inverter.

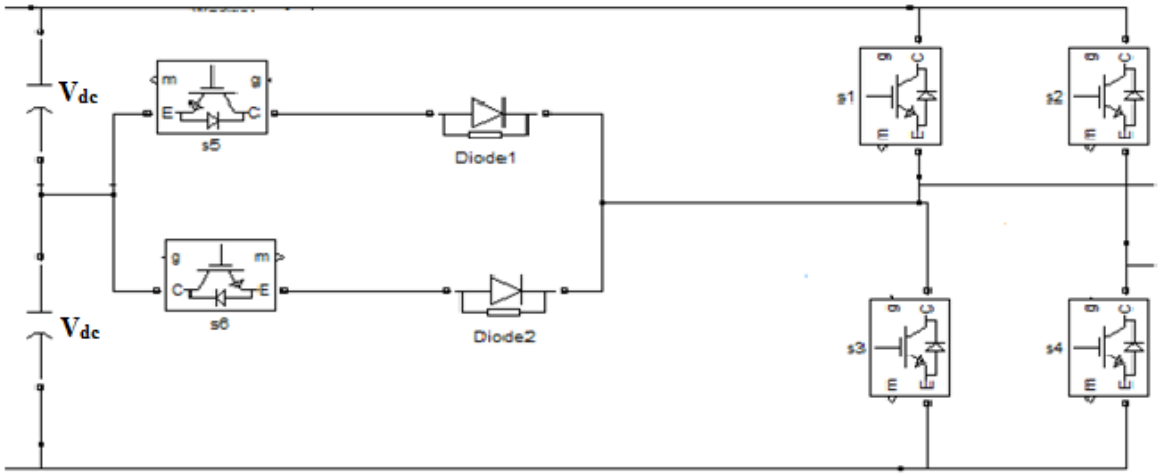


Fig 5 A

Single Phase Modified Cascaded Five Level Inverter

Table 1. SWITCHING STATES

On Switching State	V_a	V_b	$V_{ab}=V_0$
S4,S1	V_{dc}	0	$+V_{dc}$
S4,S6	$V_{dc}/2$	0	$+V_{dc}/2$
S4,S3	0	0	0
S2,S1	$V_{dc}/2$	$V_{dc}/2$	0

S2,S5	0	V_{dc}	$-V_{dc}$

ADOPTED PULSE WIDTH MODULATION

To obtain the five level PWM we compare reference sine wave with two carriers of high frequency(about 1.6kHz to 2kHz). First V_{ref}. is compared with the carrier1 and gives output +1 as V_{ref}. $>V_{c1}$ upto $\emptyset_1$.After Φ2 Vref is compared with Vc2 and similar outputs received. If Ma>.5 the output will be a five level.

Simulation of Three Level Inverter

Three phase inverter is modeled based on the theoretical concepts. Here pulse generator has been used for gate pulses where three reference wave (sine wave) and one carrier waves (triangular wave) are taken. Based on the concepts of modulation techniques, six pulses are generated. Theses pulses are given to the switches. Fig 6 represents the model of a 3-phase inverter.

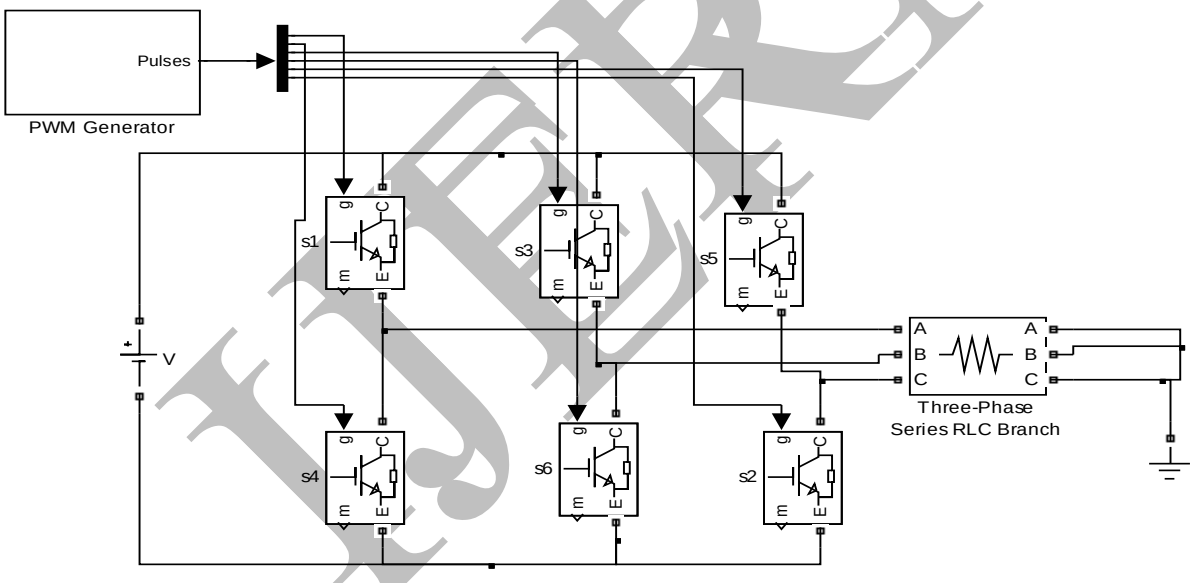


Fig 6 MATLAB/SIMULINK Model for Three Level Inverter

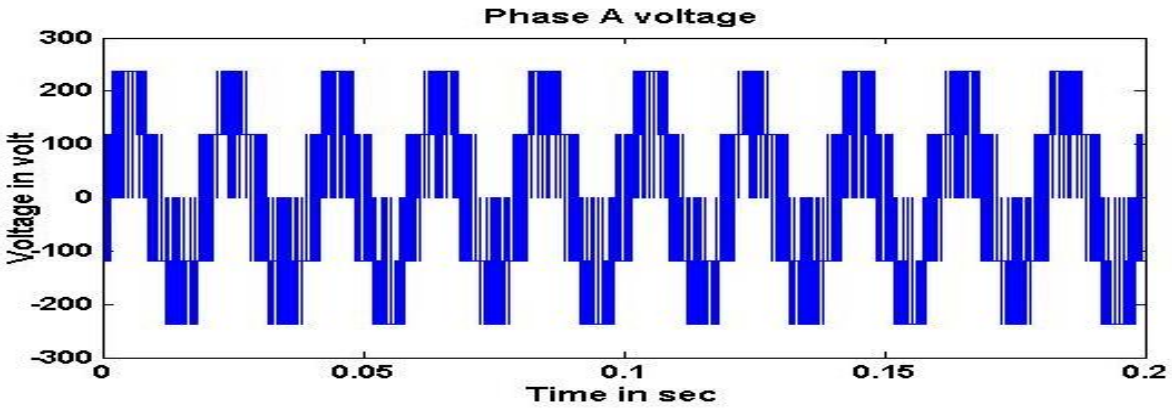


Fig 7 Phase Voltage of Three Level inverter

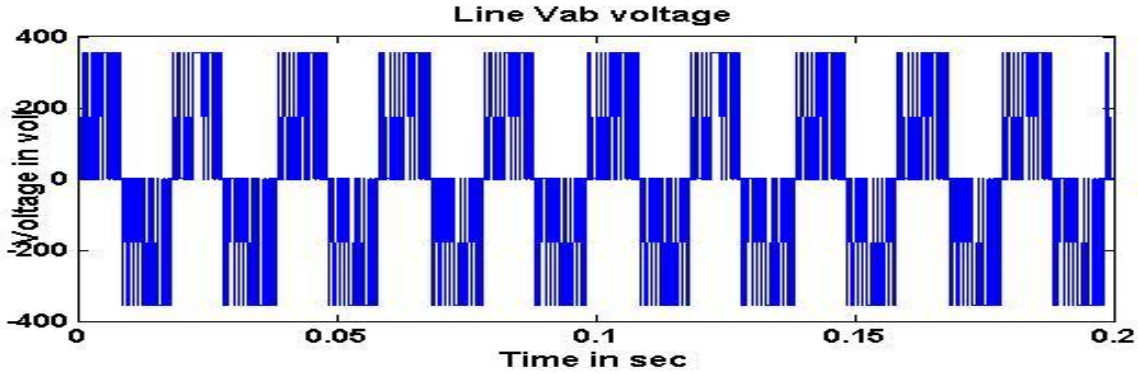


Fig 8Line Voltage of Three Level Inverter

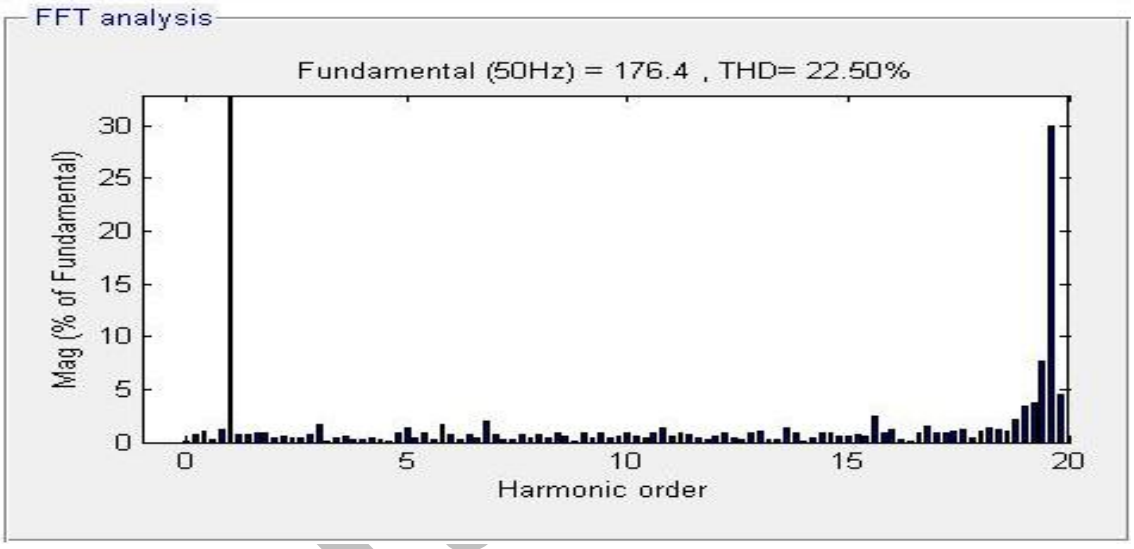


Fig 9 Harmonic Spectrum of Three Level Inverter Phase Voltage

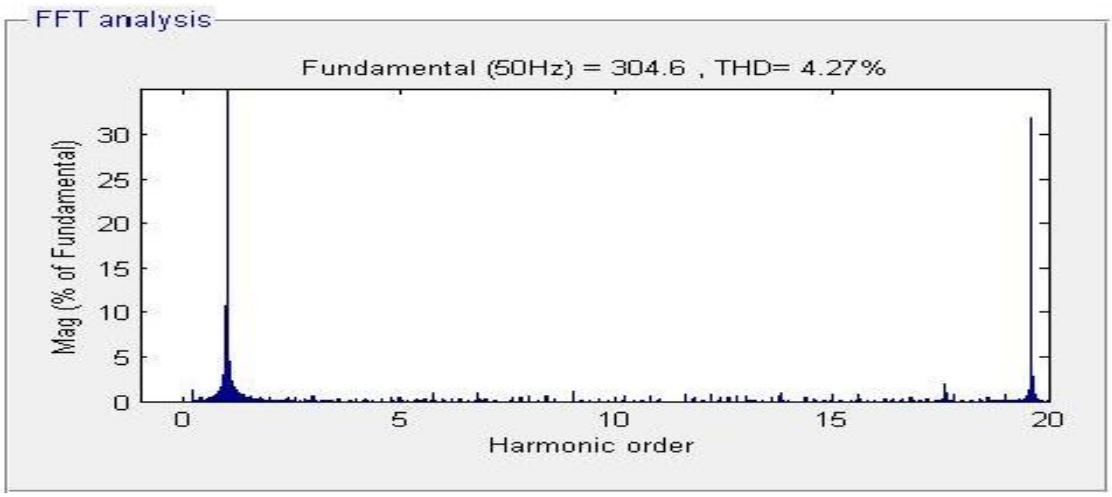


Fig 10Harmonic Spectrum of Three Phase Inverter Line Voltage

Figs. 7- 10 show the phase voltage, line voltage, & THD of a 3-level inverter. It can be observed that the total harmonic distortion (THD) for the phase voltage is 22.50% and THD for the line voltage is 4.27%.

Simulation of Modified Cascaded Five-Level Inverter

Simulation of Gate Pulses

Fig 11 shows the PWM generation for a modified cascaded five level inverter for one phase. PWM generation is considered the more important in the inverter design and several multicarrier techniques have been developed to reduce the distortion in multilevel inverters, based on the classical (SPWM) with triangular carriers.

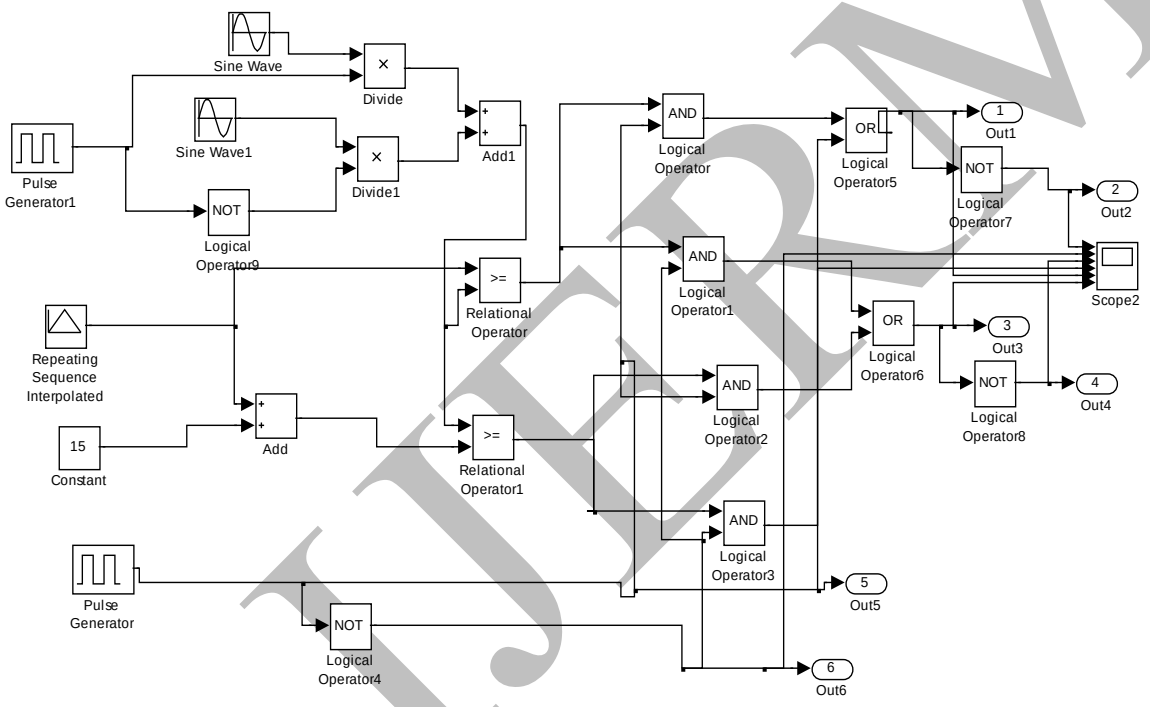


Fig 11 MATLAB/SIMULINK Model for Pulse Generation

The PWM pattern adopted in modified cascaded five level inverter makes the inverter producing output voltage with three levels (zero and half supply dc voltage positive and negative respectively) at modulation index (Ma ≤ 0.5) and five levels (zero, half and full supply voltage positive and negative respectively) at modulation index (Ma > 0.5).

Simulink Model For Modified Cascaded Five-Level Inverter

Fig 12 shows the modified cascaded five level inverter for a single phase, here an Auxiliary circuit is added in the simple H-Bridge inverter. The output voltage of simple H- Bridge inverter is the three level Voltage Waveform, to make it a five level wave the Auxiliary circuit is connected, which contains two back-to-back IGBT switches in series with the diodes. So here only six controlled switches are used to get five level which reduced the complexity of the circuit and the total harmonic distortion as compared to conventional inverter.

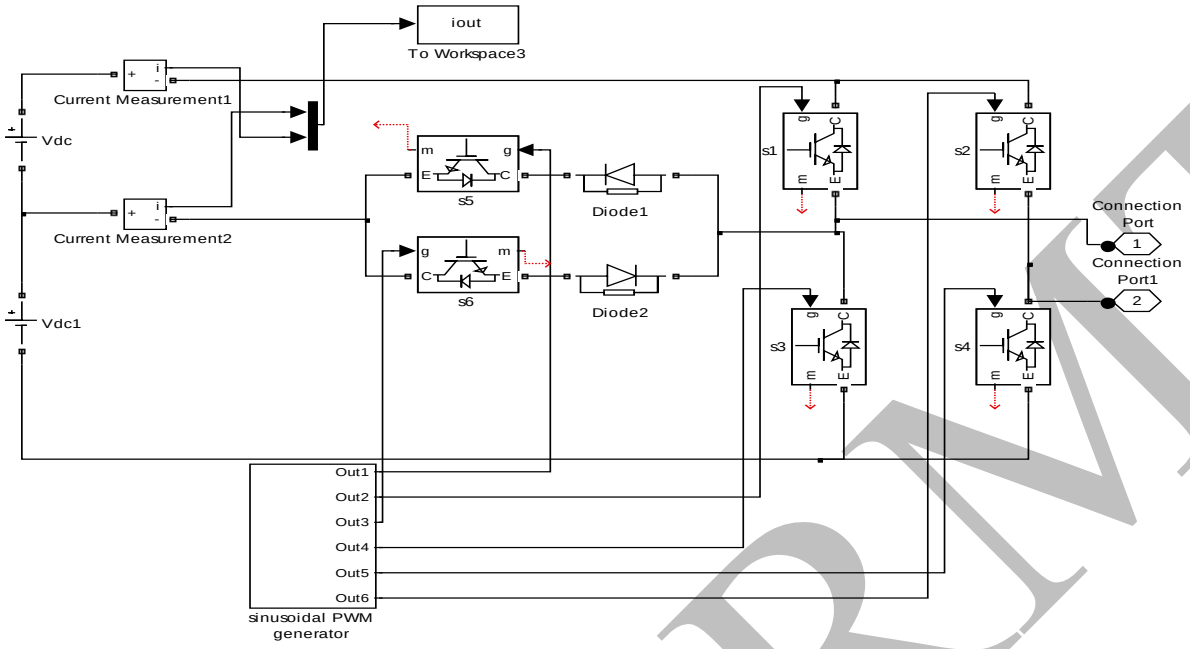


Fig 12 MATLAB/SIMULINK Model for Modified Cascaded Five-Level Inverter

Simulation Results

Figs. 13-shows the phase voltage & THD of a modified cascaded five-level inverter. By comparing the three phase inverter and a modified cascaded five level inverter we can say that the distortion in five level inverter voltage is less. The current waveforms are closed to sinusoidal. Fig 14 and 15 represents the harmonic spectrum analysis of a five level inverter. In this case, the Total Harmonic Distortion is 12.30% in phase voltage and 1.55% in line voltage. Table 4.1 shows the comparison of THD in three level inverter and modified cascaded five level inverter.

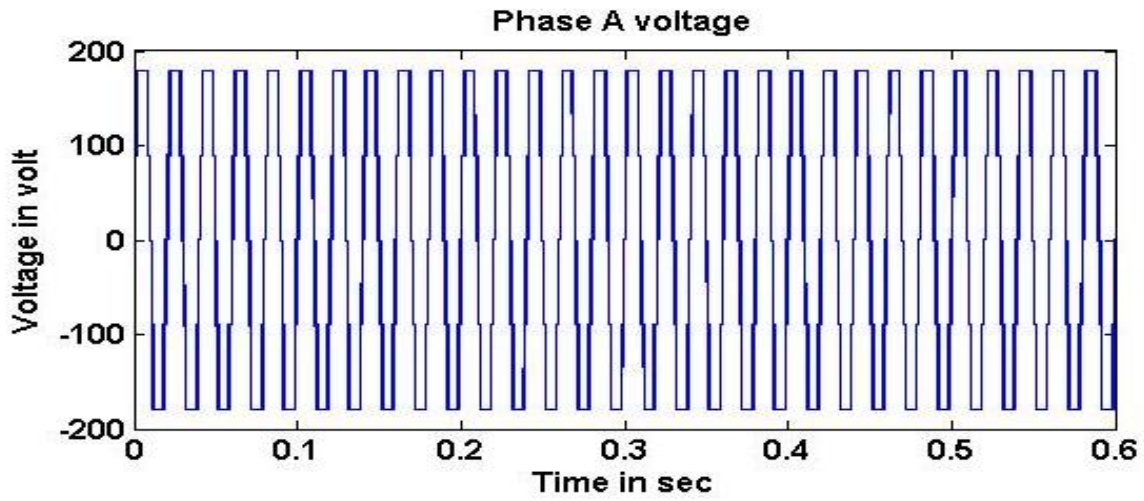


Fig 13 Phase Voltage of a Modified Cascaded Five-Level Inverter

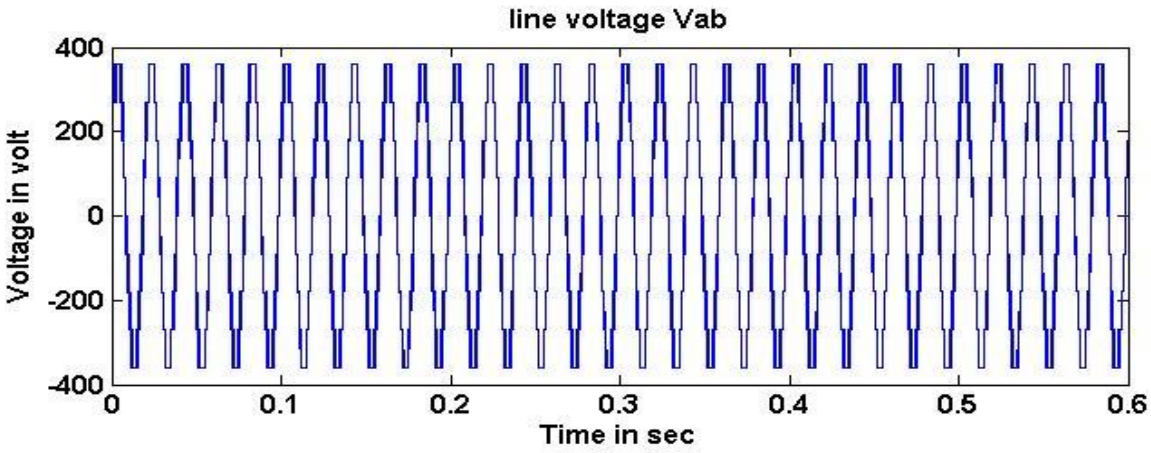


Fig 14 Line Voltage of a Modified Cascaded Five-Level Inverter

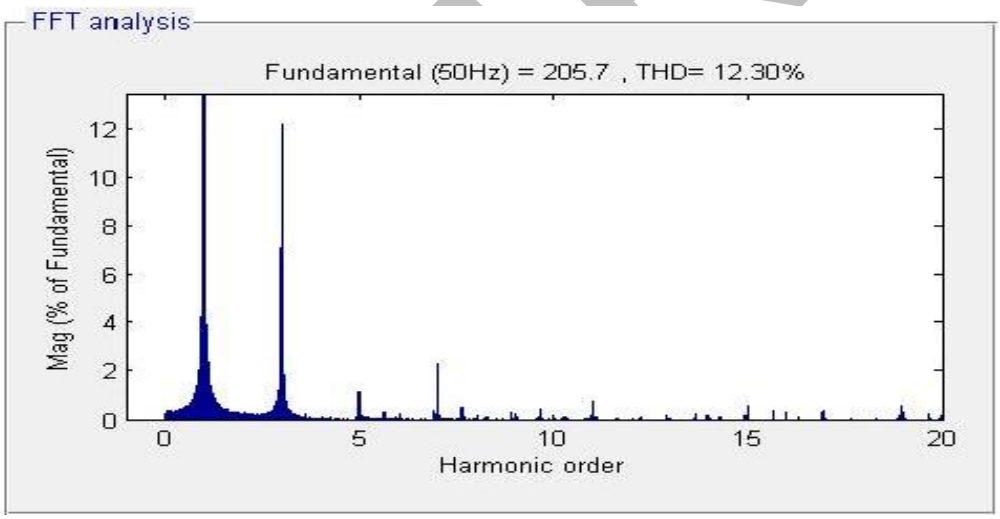


Fig 15 Harmonic Spectrum of modified cascaded Five level Inverter Phase Voltage

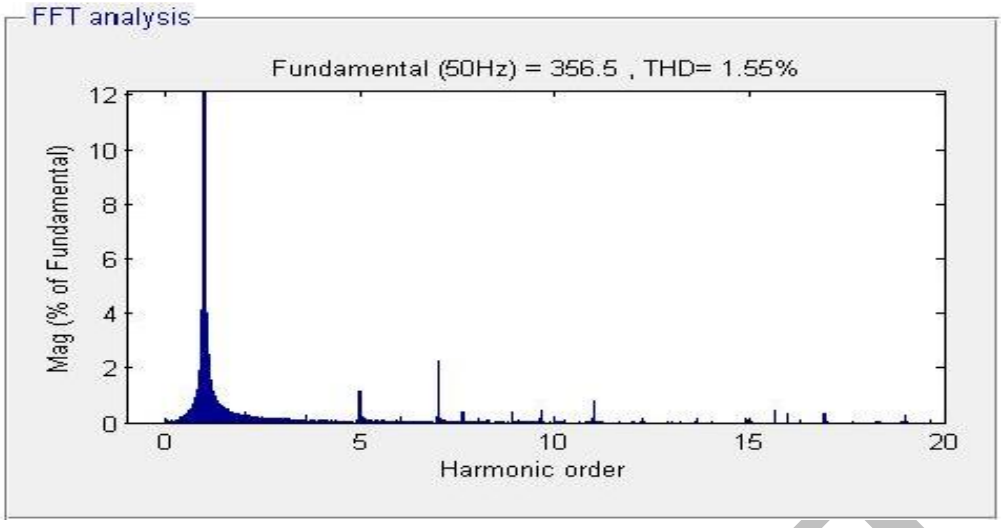


Fig 16 Harmonic Spectrum of modified cascaded Five level Inverter line Voltage

Comparison of THD of above inverter

The study gives a comparison of THD for three-phase ac output of three and five level inverter

Table 2 Comparison of THD

Parameter	THD (%) in 3- Level Inverter	THD (%) in Modified Cascaded 5-Level Inverter
PHASE VOLATGE	22.50	12.30
LINE VOLTAGE	4.27	1.55

Conclusion & Future scope

This thesis has given a brief account of multilevel inverter circuit topologies (3-level and 5-level) and their analysis with respect to induction motor drives. The THD of three level inverter and modified cascaded five level inverter has been evaluated. As based on this study the modified cascade five level inverter has less THD and gives the output voltage closer to the sinusoidal.

Each MLI has its own mix of advantages and disadvantages and for any one particular application. One topology may be more appropriate than others and the appropriate choice for best topology for a particular application may be the topic of further research. Often, topologies are chosen based on past experience, even though the chosen topology may not be the best choice for a particular application. The advantages of the body of research and familiarity within the engineering community may save many disadvantages in application. Multilevel converters can achieve more effective overall results with a switch frequency due the cancellation of the different order switch frequency terms.

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